WBG Device Reliability Team
Short-Circuit Robustness Testing of SiC Power MOSFETs

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Outline

• Introduction

• Short-Circuit Experimental Setup and Method
  • Short-circuit robustness testing according to MIL-STD-750E, Test Method 3479

• Results and Analysis
  • Critical energy density and short-circuit withstand times
  • Observed failure modes

• Conclusion
• Unintentional short-circuits occur in power electronic converters

• High power dissipation can destroy the device when the junction temperature exceeds its rated value

• Protection circuitry is required to turn-off short-circuit to avoid device destruction

• MOSFETs must provide sufficient ruggedness to withstand high short-circuit currents at high DC link voltages

T. Shoji, et. Al, R&D Review of Toyota CRDL Vol. 39 No. 4
**Introduction**

Existing trend is to drive down $R_{on,sp}$ by scaling planar DMOSFET or go to trench-gate design.

- Is a measure of the current handling capability for a given die size
- The smaller the value, the smaller you can shrink the die
- Smaller die size lowers the cost
- Better switching performance due to lower gate charge

How is robustness and reliability affected?

- Submicron channel length and small cell pitch increases SC current and reduces SC withstand time

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Experimental Setup and Method

**Figure 3479-1. Test circuit**

**Figure 3479-2. Short-circuit withstand time waveform.**

Short-circuit failure modes in Si Power IGBTs
Experimental Results

- Peak short-circuit current (A)
- DC link voltage, $V_{\text{DC}}$ (V)
- MOSFET-C
- MOSFET-A
- MOSFET-B

$V_{\text{GS}} = 20.0 \text{ V}$
$T_{\text{PW}} = 2.5 \text{ us}$
Experimental Results

Observed reduction in $V_{GS}$ is precursor to failure

- Gate oxide is designed thinner for SiC in comparison to Si planar MOSFETs

- Under extreme operating mode this could be a reliability problem

- Most manufacturers have implemented a shielded planar structure which is supposed to have better reliability

- $V_{GS}$ reduction attributed to increase in gate leakage current

Experimental Results

Different failure modes observed between COTs MOSFETs A and B:

- MOSFET-A failed catastrophically with G-S and D-S short
- MOSFET-B has delayed G-S failure
- MOSFET-C is a developmental device and failed catastrophically
- Short-circuit withstand time, $t_{sc}$ observed for MOSFET-A and MOSFET-B are 8 µs and 13 µs, respectively.

Destructive failure of device A at $t_{sc} = 8$ µs, $V_{DS} = 600$ V, $V_{GS} = 20$ V, and $T = 25$ °C

Destructive failure of device C at $t_{sc} = 7$ µs, $V_{DS} = 600$ V, $V_{GS} = 20$ V, and $T = 25$ °C

Device B has soft gate failure (not captured) after successful turnoff at $t_{sc} = 13$ µs, $V_{DS} = 600$ V, $V_{GS} = 20$ V, and $T = 25$ °C
Short-circuit energy density

- MOSFET-B
- TCAD Simulation
- MOSFET-C
- MOSFET-A

Short-circuit energy density (J/cm²) vs. Ambient temperature (K)
Short-circuit withstand time

Generating data < 600 V

Data presented by Stephen Arthur GE During SiC MOS Program Review 2015

DC link voltage, $V_{DC}$ (V)

Short-circuit withstand time (μs)
The short-circuit robustness is different between the various manufacturer devices.

Different failure modes were identified between the two major suppliers of SiC power DMOSFETs.

Destructive failure of MOSFET-A but MOSFET-B failed soft with G-S short.

Use structural analysis to investigate soft gate fails and correlate to electrical data.