Next Generation SiC MOSFETs
Performance and Reliability

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Grider, Jeff Casady, Al Burk, Michael O’Loughlin,
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• The Wolfspeed division to be acquired includes:
  - The Power and RF device business
  - The SiC substrate business for Power, RF and gemstone applications

• The LED portion of Cree’s Materials business will remain part of Cree

• We remain and operate as separate companies until the transaction closes

• It is business as usual for us until the transaction closes

• The transaction is subject to US Government regulatory approval and is expected to close within calendar year 2016.
ACKNOWLEDGEMENTS

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OUTLINE

• Wolfspeed SiC MOSFET Product Portfolio
  — Design principles and evolution of device generations

• Introduction to Trench MOSFETs for next generation

• Performance and Reliability
  — 900V/10 mΩ Gen 3 MOSFETs
  — Intrinsic Failure Mode High Voltage and Gate Lifetime Estimates
  — Gate Qualifications and Attempting to Predict Early Failures

• Summary
MOSFET RESISTANCE

• Channel resistance is a significant portion of resistance in lower voltage products
• Cell pitch drives channel packing density – the higher the channel density, the lower the total channel resistance ($R_{ch}$)
• Proper Engineering of the JFET gap reduces JFET resistance ($R_{JFET}$) while improving the shielding of the gate oxide
SPECIFIC ON-RESISTANCE AND BREAKDOWN VOLTAGE

- 1-D Limit $\rightarrow$ Epitaxy Capability
- Achieved the limit for 3.3 kV and higher SiC DMOSFETs
- Gains remain to be had for lower voltage SiC DMOSFET products
  - Increase channel density
  - Increase channel mobility
1200V PLANAR MOSFET ON-RESISTANCE EVOLUTION

Optimized Epitaxy, reduced cell pitch, cell engineering

Specific On Resistance (mΩ cm²)

<table>
<thead>
<tr>
<th>Generation</th>
<th>Description</th>
<th>25°C</th>
<th>150°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen 1</td>
<td>Planar (2011 Product)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gen 2</td>
<td>Planar (2013 Product)</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Gen 3</td>
<td>Planar (2016 R&amp;D)</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>0.8X Gen 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.5X Gen 1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TRENCH MOSFET – INCREASED CHANNEL DENSITY

Cell Pitch

Planar MOSFET

Specific On Resistance (mΩ cm²)
0 2 4 6 8 10 12

Gen 1 - Planar (2011 Product)
Gen 2 - Planar (2013 Product)
Gen 3 - Planar (2016 R&D)
Gen 4 - Trench (Est)

Reaching practical limits

Must demonstrate equivalent or better reliability in going from Planar to Trench geometry

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PERFORMANCE AND RELIABILITY UPDATE
RELIABILITY REQUIREMENTS

• Large segment of the potential market driven by high power applications, requiring many chips in parallel
  — Solar Inverters
  — Industrial Drives and Power Supplies
  — EV Drives

• Need to drive to PPM failure rates or better

900V/2.5 mΩ Half Bridge Module
4x 900V/10 mΩ MOSFETs per switch position
MOTIVATION FOR SiC IN EV DRIVES

- Assume Ford Focus EV equipped with 90kW IPM motor
- C-Max 90kW Si IGBT inverter or Wolfspeed 88kW SiC inverter as the traction drive
- Synchronous rectification of SiC devices; no diodes in parallel with SiC MOSFETs

Compared with Si inverter, SiC reduces inverter losses ~67% in combined EPA drive cycle
BENCHMARK 900V SiC & 650V Si (IGBT) POWER MODULES

- 900V SiC XAB350M09HM3 compared with 650 V EconoDUAL3 Si IGBT
- 250 V higher blocking voltage
- 10-20x lower body diode recovery, gate charge, and reverse transfer capacitance.
- Symmetrical 3rd quadrant conduction
- Lower on-state losses

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Wolfspeed XAB350M09HM3</th>
<th>silicon FF450R07ME4_B11</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>HT-3000 (custom)</td>
<td>EconoDUAL3™</td>
</tr>
<tr>
<td>Blocking voltage (V)</td>
<td>900</td>
<td>650</td>
</tr>
<tr>
<td>$T_{J,\text{MAX}}$ (°C)</td>
<td>175</td>
<td>150</td>
</tr>
<tr>
<td>$R_{DS,\text{ON}}$ (mΩ) (25°C/150°C)</td>
<td>2.5 / 3.6</td>
<td>N/A</td>
</tr>
<tr>
<td>$I_{DS} @ 150°C$ (A)</td>
<td>405</td>
<td>430</td>
</tr>
<tr>
<td>$Q_G$ (nC)</td>
<td>648</td>
<td>4800</td>
</tr>
<tr>
<td>$Q_R @ 150°C$ (nC)</td>
<td>2.02 (0.504 x 4)</td>
<td>35.5</td>
</tr>
<tr>
<td>Input capacitance, $C_{iss}/C_{ies}$ (nF)</td>
<td>15.7 (3.93 x 4)</td>
<td>27.5</td>
</tr>
<tr>
<td>Rev. transfer cap, $C_{rss}/C_{res}$ (pF)</td>
<td>72 (18pF x 4)</td>
<td>820</td>
</tr>
</tbody>
</table>
Accelerated Life Testing under High Temperature Reverse Bias Conditions (ALT-HTRB)

- 150°C
- Drain Bias Conditions: 1460V, 1540V, 1620V
- Test to Failure
- Collate Failure Time Statistics

Extrapolated Mean Time to Failure at 800V
30 Million Hours
3400 Years
ALT-HTRB – 900V/65 mΩ GEN 3 MOSFETS

C3M0065090D MOSFETs – 900V/65mΩ
• 60 Devices
• Parts Run for >1800 hours at 150°C at 1200V+
• Three failures from the population as of 1800 hours
HV LIFETIME PROJECTIONS FOR 900V/65 mΩ GEN 3 MOSFETS

- 900V rating results in 65 years before the first projected 1% of failures
- Avalanche rated: zero fails in 1,000 hours at 50 μA, V > 1200V
GATE LIFETIME PROJECTIONS FOR 900V/65 mΩ GEN 3 MOSFETS

- Extrapolated Intrinsic $V_{GS}$ lifetime of ~600M hours at +15V (DC recommended operating point)
- Passed AEC-Q101 qualification of 3 lots x 77 parts with Ø fails in 1,000 hrs at $V_{GS}=15V, 150C$
## HIGH TEMPERATURE GATE BIAS QUALIFICATIONS

<table>
<thead>
<tr>
<th>Part Type</th>
<th>Sample Size</th>
<th>Total Area Tested</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>900V/65mΩ Gen 3</td>
<td>3x77 = 231*</td>
<td>790 mm²</td>
<td>150°C, 15V, 1000 hrs</td>
</tr>
<tr>
<td>1200V/25mΩ Gen 2</td>
<td>3x25 = 75</td>
<td>1380 mm²</td>
<td>150°C, 20V, 1000 hrs</td>
</tr>
<tr>
<td>1200V/25mΩ Gen 2</td>
<td>3x25 = 75</td>
<td>1380 mm²</td>
<td>175°C, 20V, 1000 hrs</td>
</tr>
<tr>
<td>1700V/45mΩ Gen 2</td>
<td>3x25 = 75</td>
<td>1660 mm²</td>
<td>150°C, 20V, 1000 hrs</td>
</tr>
<tr>
<td>1700V/45mΩ Gen 2</td>
<td>3x25 = 75</td>
<td>1660 mm²</td>
<td>175°C, 20V, 1000 hrs</td>
</tr>
<tr>
<td>CAS300 Module 1200V/25mΩ Gen 2</td>
<td>6 switches x 6 die/s</td>
<td>665 mm²</td>
<td>125°C (limited by module housing), 20V, 1000 hrs</td>
</tr>
</tbody>
</table>

* Full AEC-Q101 Qualification to meet Automotive Qualification Standards

- 7500 mm² total die area tested
- Equivalent of 1,200 of C2M0080120D (1200V/80 mΩ Gen 2) MOSFETs tested for 1000 hours with zero failures
ACCELERATED HTGB

<table>
<thead>
<tr>
<th>Part Type</th>
<th>Sample Size</th>
<th>Total Area Tested</th>
<th>Conditions</th>
<th>Elapsed Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1200V/25mΩ Gen 2</td>
<td>290</td>
<td>5350 mm²</td>
<td>175°C, 27V (20V $V_{use}$)</td>
<td>1000 Hours, 0 Fails</td>
</tr>
<tr>
<td>900V/10mΩ Gen 3</td>
<td>240</td>
<td>5540 mm²</td>
<td>175°C, 20V (15V $V_{use}$)</td>
<td>800 Hours (and counting), 0 Fails</td>
</tr>
</tbody>
</table>

Assuming a voltage acceleration factor of 4.0 cm/MV:

- A Gen 2 MOSFET that survives for 1000 hours at $V_{GS} = 27V$ is estimated to survive for 50 years at $V_{GS} = 20V$
- A Gen 3 MOSFET that survives for 800 hours at $V_{GS} = 20V$ is estimated to survive for 21 years at $V_{GS} = 15V$
SUMMARY

• At Voltage ratings ≤ 3.3 kV, channel resistance becomes a significant fraction of total device resistance
  — We continue to drive to higher cell density and optimized epitaxy of our Planar DMOSFET technology to drive to more efficient MOSFET products
  — We are approaching the limits of the planar technology, but there is one more generation of device that we can achieve

• Any forthcoming technology must match the reliability of the Planar DMOSFET platform

• Intrinsic Reliability is superb, but we will continue to examine defectivity and accelerated test conditions to drive failure rates down on large populations of parts

• We have demonstrated T1% Lifetimes of greater than 50 years (Gate Lifetime and High Drain Bias Lifetime)