SiC MOSFET Activities at GE & PEMC

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Outline

- Devices
- Reliability
- PEMC
Comparison of 1.2kV SiC MOSFETs
GE delivers best in class performance across temp. range

Device current rating:

\[
I_D = \sqrt{\frac{T_{\text{max}} - T_{\text{case}}}{R_{\theta_{\text{max}}} \times R_{\text{On}_{\text{max}} @ T_{\text{max}}}}}
\]

\[
I_D, 125^\circ C = \sqrt{\frac{200 - 125}{0.75 \times 0.090}}
\]

\[
I_D, 125^\circ C = 33A \Rightarrow 30A \text{ rating}
\]

<table>
<thead>
<tr>
<th>Device</th>
<th>Die Area (cm²)</th>
<th>( R_{\text{On}} ) Typ. @ Irated 25°C</th>
<th>( R_{\text{On}} ) Typ. @ Irated 150°C</th>
<th>( R_{\text{On}} @ 150^\circ C \times \text{Die Area} ) (mOhm·cm²)</th>
<th>( R_{\text{On}} ) Typ. @ Irated 200°C</th>
<th>( R_{\text{On}} @ 200^\circ C \times \text{Die Area} ) (mOhm·cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vendor 1 COTS</td>
<td>0.104</td>
<td>80m</td>
<td>145m</td>
<td>15.1</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Vendor 2 COTS</td>
<td>0.134</td>
<td>80m</td>
<td>135m</td>
<td>18.1</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>GE (2015)</td>
<td>0.101</td>
<td>54m</td>
<td>72m</td>
<td>7.3</td>
<td>90m</td>
<td>9.1</td>
</tr>
<tr>
<td>2015 GE SiC MOSFETs: ((R_{\text{On}} @ 25^\circ C / R_{\text{On}} @ 150^\circ C))</td>
<td>45mΩ/75mΩ, 1.2kV</td>
<td>20mΩ/45mΩ, 1.7kV</td>
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<tr>
<td>2016 GE SiC MOSFETs: ((R_{\text{On}} @ 25^\circ C / R_{\text{On}} @ 150^\circ C))</td>
<td>20mΩ/45mΩ, 1.2kV</td>
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<td></td>
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* P. Losee et al. “1.2kV Class SiC MOSFETs with Improved Performance over Wide Operating Temperature,” 2014 ISPSD
1.2kV, 30A MOSFET Avalanche Ruggedness

Superior to silicon:
900V/23A Si CoolMOS™: $E_a < 4 \text{J/cm}^2$

GE12N20L SiC MOSFET: $E_a > 15 \text{J/cm}^2$

Tight distribution of $E_{AV}$ is an indication of excellent design-process robustness
1.2kV, 30A Short-Circuit Capability

- SC capability important for system safety
- SC capability established for GE 1200V/30A MOSFET
- $t_{sc} \approx 10\,\mu s @600V \rightarrow$ sufficient for fault detection to react
- GE12N20L SC test example:
Reliability
SiC MOSFET $V_{TH}$ Stability

- **Negative Bias Threshold Instability (NBTI)**
  
  Stressed at $V_{GS} = -15V / T = 200^\circ C$

  - **Vendor 2 SiC MOSFET**
  - **Vendor 1 SiC MOSFET**

  - Normally-on after 70 hrs

- **Positive Bias Threshold Instability (PBTI)**

  $V_{TH}$ stability => 200$^\circ$C rating

$V_{TH}$ Stability enables 200$^\circ$C Rating
GE MOSFET Lifetime Model, Gate FIT Rate

Lifetime Model Based on Accelerated Stress Testing of 1.2kV, 30A MOSFETs

- **Lifetime**: \( T_{LIFE,63\%} = e^{\alpha_0 + \alpha_1 \times E_{FIELD} + \alpha_2 / kT} \)
- \( T_{LIFE,63\%} \) relates stress test to use conditions
- **Acceleration factor**: \( AF = \frac{T_{LIFE,63\% @ use\ conditions}}{T_{LIFE,63\% @ test\ conditions}} \)
- Third-party testing validated both the model and the gate reliability
1.2kV, 30A SiC MOSFET Gate Failure Rate

Gate failure rate at use conditions: \( V_{GS} = 20V, T_j = 150\degree C \)
with 90\% confidence intervals:

Model predicts that GE SiC MOSFET failure rate FIT < 10 (less than ten failures per billion device-hours) meets system requirements.
200°C SiC MOSFET Qualification
1.2kV, 30A TO247 part qualified per AEC-Q101

Pass/fail criteria:
- $D_{V_{TH}} = +/- 20\%$ Max
- $D_{R_{ON}} = +/- 20\%$ Max
- $D_{L_{DSS,1200}} < 5x$ Max

$\rightarrow 0/77$ failures

**HTGB:** 1000 hr, 200°C, $V_{GS}=23V$:
- Passed

**HTRB:** 1000 hr, 200°C, $V_{DS}=960V$:
- Passed

1000 temp. cycles (-55 to +200°C):
- Passed

*P. Losee et al. “1.2kV Class SiC MOSFETs with Improved Performance over Wide Operating Temperature,” 2014 ISPSD*
Technical applications (e.g. aerospace) prioritize performance ahead of other requirements demanding higher switching frequency, power density, and operating temp and set some of our reliability requirements.

Industrial application emphasize low cost & high reliability with an aversion to unproven technology due to the possible high cost of lost productivity and the large number of devices per module/system. They need device failure rates below 10 FITs, while maximizing power output.

GE data suggests that the technology is ready for insertion, how to do this at scale & cost beyond what is possible at the GRC facility?
NY Governor Andrew M. Cuomo announced that NYS will partner with private companies, led by GE, to launch the New York Power Electronics Manufacturing Consortium (NY-PEMC). $250+ million investment for Silicon Carbide

NY-PEMC will enable and support industrial partners to:

- Develop next gen materials and processes for wide band gap (WBG) semiconductors;
- Create thousands of high-skilled, high-paying jobs focusing on the development and manufacture of next gen WBG semiconductors used in power devices; and
- Leverage and operate through the successful SUNY Polytechnic Institute public-private partnership model to allow burden sharing and enable rapid growth of emerging technologies in diverse application spaces i.e. transportation, aviation, smart grid
Advantages and Applications of silicon carbide (SiC) power devices

**Higher max. temperature:**
\[ T_{\text{SiC}} \geq 200^\circ C \] vs. \[ T_{\text{Si}} \leq 175^\circ C \]

**Reduced power losses...**
by more than 50%

**2X higher power density...**
more compact / powerful

**More reliable in high temperature environments**

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**Silicon carbide vs. current devices**—will save enough electricity to power the entire state of New York.

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**Driving the next power revolution**

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**Oil and Gas**
More efficient motors that perform in hotter, harsher environments to enhance oil recovery

**Hybrid Vehicles**
10% longer driving range (e.g., additional 400 miles on a car averaging 40 miles per gallon)

**Medical Imaging**
Smaller, more efficient systems to lower the cost of healthcare, free up valuable hospital floor space

**Data Centers**
>5% energy savings for fastest growing segment of electricity consumption

**Airplanes**
Reduce weight by 1,000 lbs. with more compact, high efficiency power systems

**Renewables**
More clean energy, 50% reduction in wasted power

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**GE’s Advanced Silicon Carbide Power Semiconductors**
Integrated and growing team of 35 GE (20) and SUNY Poly (15) engineers and staff members focusing on the installation of a bridge 6” SiC line

Manufacturing equipment will be specified as 200mm, capable of processing 150mm SiC wafers

Ultimate SiC production output up to 50,000 wafers/year

Class 100 cleanroom processing area with proper ESD controls

MES managed processing facility under ISO 9001 Quality system

Full complement of metrology and analytical equipment suite
SUNY Poly is Experienced in Consortium Management

- **G450C** is transitioning the industry from 300mm to 450mm wafers
  - Significant public - private investment
  - Multi-national member companies – IBM, Intel, TSMC, GlobalFoundries, Samsung
- **U.S. PVMC** – Thin Film PV Solar, scaling roll-to-roll processing from .3m to 1m
  - >40 Industrial and research members
- **IBM Joint Development Alliance** – 300mm
  - Multi-national member companies – ST, Infineon, Renesas, Toshiba, GlobalFoundries, Samsung
- SUNY Poly provides leadership, unique IP protection, cooperation, state-of-the-art shared use facilities, and burden sharing
World Class Facilities

NanoFab 300/450 Extension
NanoFab 300 South & South Annex
NanoFab 300 North – SiC Line
NanoFab 300 Central
NanoFab East
ZEN Building
CESTM
SUNY Poly State-of-the-Art 300mm Facilities in NanoFab 300 North
PEMC Fab Attributes

1) Fab is SiC dedicated, no silicon except for metrology

2) SiC fab is a “clean sheet” design, based on ≥200 mm silicon tools & some unique SiC tools
   - 200 mm capable when needed
   - Tools have high degree of automation
   - Tools are clean by design (e.g. internal ULPA filters & ESD control)

3) Fab tools were selected with a proven MOSFET baseline process in mind

4) In line metrology tools for fab control are part of the design philosophy (defect & particle control)

5) Feedback of device results are immediate (yield, reliability, parametric performance..), to shorten learning cycles
• Qualified 1.2kV MOSFET baseline SiC process capability
• Parametric Test and Dice capability.
Baseline Process Based on Proven GE MOSFET Device Process Flow

Alignment Marks

P-Well Implant

N-plus Implant

P-plus Implant

P-JTE Implant

Activation

Field Oxide

Gate

Inter-Layer Dielectric

Ohmic Contacts

Gate Pad

Pad Metal

Passivation

Backmetal

Polyimide
Four Pillars of NY-PEMC Activities

Fabrication

Design, Modeling & Feasibility
- Existing SiC Fab (Industry and Universities)
- Enablement for Device SMEs & OEM Development
- Design & Modeling

MRL 7-10

Devices from Partners

Post Fabrication
- Packaging
- Testing & Characterization
- Reliability

System
- HVDC / MVDC
- MV Motor Drive
- PV Inverter
- Wind Converter
- Data Center
- Aviation
- EV Charger
- DC-DC

MRL 7-10

SiC
- 6” Installation/Fit Up | 2015
- 6” Qualification | 2016
- 6” Production | 2017

Application Development & Demonstration
- Parametric testing for SiC MOSFETs, JFETs, IGBTs, diodes, and thyristors
- Wide range of SiC testing capabilities
- 100 ~ 200 mm SiC wafers
- 5000 V / 100 A capability
- Cassette-to-cassette testing
- Automatic data transfer & analysis
- Room temp to 250°C wafer chuck
- Fully automatic wafer-level TDDB reliability test for MOSFETs & IGBTs
- High temp 250˚C and higher voltage failure rate acceleration
- Failure rate analysis (time zero, extrinsic, intrinsic failure)
~$200M of Metrology & Analysis
Capabilities Available to NY- PEMC

Inline Inspections & Metrology, Electrical & HV Tests, Reliability

Sample Preparation
- FIB & Lamella extraction
- Polishing
- Plasma cleaning
- Micro RIE

Electrical Characterization
- Parametric test
- Hall measurement
- Four Point Probe
- Interface / Traps evaluation
- Cryogenic measurements
- High frequency and noise measurements

Electron and Optical Microscopy
- TEM
- SEM
- Ellipsometry
- Photoluminescence
- Raman

Surface and Structure Analysis
- AES
- Dynamic and TOF SIMS
- XPS
- RBS, PIXE, NRA
- AFM and Profilometry
- XRD, XRR, HRXRD

Offline Metrology and Physical Analysis

Process Optimization and Failure Analysis

Inline Characterization and Metrology
- Specialized SiC Defect Inspection – Epi and Patterned inspection
- Four Point Probe
- Profilometry
- Spectral Ellipsometry
- Patterned Defect Inspection
- SEM Defect review & EDS
- TDDB characterization
- TXRF and KLA SP1
- Film stress
- Yield management software
NY-PEMC SiC Timeline

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<tbody>
<tr>
<td>Tool Set Selected</td>
<td>RFP and PO process</td>
<td>Equipment Installation</td>
<td>Process Verification</td>
<td>1st SiC MOSFET</td>
</tr>
<tr>
<td>Fab Prep</td>
<td></td>
<td></td>
<td></td>
<td>ISO certified</td>
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<tr>
<td></td>
<td>MOSFET yield, reliability optimization</td>
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<td>Qualified SiC MOSFET</td>
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There are multiple methods of engagement:

1. Purchase GE designed MOSFET wafers and/or devices
2. Use of NY-PEMC Line as Foundry
3. Customize GE MOSFET for Company use
4. Proprietary access to NY-PEMC facilities
5. Collaborative access to NY-PEMC programs
Active Engagement with NY-PEMC Provides Companies:

- Access to new partnerships with supply chain companies, SMEs and start-ups, application specific companies, as well as large multinational customers and vendors
- Ability to participate in and define and drive consortial activities that are in Company’s best interests, i.e. reliability
- Potential to coordinate and drive vertical alignment with existing Company partners or new ones from NY-PEMC
- Access to an ISO 9001 certified and AEC-Q101 compliant tool set
- Ability to develop new packaging solutions for current and future applications
- Ability to access a wide range of NYS tax and funding incentives, including
NY-PEMC Points of contact:

- Joseph Alteri
  Assistant Vice President, Business Development and Economic Outreach
  Info.ny-pemc@sunypoly.edu
  (518) 956-7147

- Paul Kelly
  Associate Vice President for Consortia Programs and Initiatives
 Pkelly2@sunypoly.edu
  518-788-9538 or
  518-956-7392

- Web Information at : www.ny-pemc.org
SiC driving the next power revolution

Higher efficiency AND higher power density

- Server PS: > 5% datacenter-level energy savings
- UPS: > 5%, datacenter-level energy savings footprint -25%
- PV inverter: > 50% lower losses
- Wind converter: > 50% lower losses
- Aircraft electric power: 500kg lower weight
- Electric locomotive: 5% lower weight
- MV motor drive: > 25% smaller footprint
- Electric propulsion: ~ 10% less fuel consumed

New capabilities

- Ship electric power distribution: 10x lower transformer weight
- MRI, CT: better image quality, smaller footprint
- MV/HV grid applications: 3X fewer devices for SiC vs. Si
- Oil and gas: New capability in hot & harsh conditions

Applications range from KW to MW

Target system opportunities being explored with GE SiC MOSFETs. PEMC is a mechanism through which this technology will be enabled within GE and available to others.
END